Amendments to the Claims

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended)   Circuit testing equipment comprising;

a computer having stored thereon a boundary scan description language (BSDL) file, a netlist and a connections list; and

a connector for connecting the computer to a boundary scan bus of a circuit to be tested, the circuit to be tested, <u>the circuit to be tested having at least one integrated circuit</u>;

the computer being arranged to parse the BSDL file, the netlist and the connections list and generate a data structure therefrom which, when combined with a test script <u>associated with the integrated circuit</u>, permits execution of the test script from the computer through the boundary scan bus.

2. (Currently Amended)   The equipment of claim 1 <u>for testing a first pin of a first device of the circuit to be tested</u>, wherein the computer has all information necessary to identify whether, for a ~~given~~ <u>the first</u> pin, a BSDL file is present and whether the ~~given~~ <u>first</u> pin is connected through the netlist to a <u>second</u> pin of a <u>second</u> device for which a BSDL file is present, whereby the <u>first</u>, pin can be controlled using the boundary scan bus.

3. (Currently Amended)   Equipment according to claim 1, wherein the computer comprises a parser for parsing the BSDL file, the netlist and the connections <u>list</u>, and a compiler for compiling the same to generate the data structure for execution with the test script.

4. (original)   Equipment according to claim 1, wherein the computer further comprises at least one test script for testing an integrated circuit of the circuit to be tested.

5. (original)   Equipment according to claim 4, wherein the integrated circuit has pins that are

capable of adopting one of three states, being a high state, a low state and an input state, and wherein the test script is arranged to sequentially test whether a pin is in a read state by testing whether it can sequentially be driven into the low state and the high state.

6. (original) Equipment according to claim 1, wherein the computer further comprises a first test script for testing a first integrated circuit of the circuit to be tested and a second test script for testing a second integrated circuit of the circuit to be tested.

7. (original) Circuit testing equipment according to claim 1 for testing a circuit that has at least one first integrated circuit (IC) that is boundary-scan capable and at least one second IC that is not boundary-scan capable, wherein the data structure defines all pins of the first IC that are capable of driving pins of the second IC and all pins of the first IC that are capable of reading pins of the second IC, whereby the second IC and its connections to the first IC can be tested by driving pins of the first IC.

8. (Currently Amended) Circuit testing equipment for testing a circuit that has at least one first integrated circuit (IC) that is boundary-scan capable, and at least one second IC that is not boundary-scan capable, the equipment comprising:

an input for inputting files comprising a boundary scan description language (BSDL) file, a netlist and a connections list; and

a data structure generated from the BSDL file, the netlist and the connections list that defines all pins of the first IC that are capable of driving pins of the second IC and all pins of the first IC that are capable of reading pins of the second IC, whereby the second IC and its connections to the first IC can be tested by driving pins of the first IC using a test script that is specific to me second IC but independent of the first IC.

capable of adopting one of three states, being a high state, a low state and an input state, and wherein the test script is arranged to sequentially test whether a pin is in a read state by testing whether it can sequentially be driven into the low state and the high state.

6. (original)   Equipment according to claim 1, wherein the computer further comprises a first test script for testing a first integrated circuit of the circuit to be tested and a second test script for testing a second integrated circuit of the circuit to be tested.

7. (original)   Circuit testing equipment according to claim 1 for testing a circuit that has at least one first integrated circuit (IC) that is boundary-scan capable and at least one second IC that is not boundary-scan capable, wherein the data structure defines all pins of the first IC that are capable of driving pins of the second IC and all pins of the first IC that are capable of reading pins of the second IC, whereby the second IC and its connections to the first IC can be tested by driving pins of the first IC.

8. (Currently Amended)   Circuit testing equipment for testing a circuit that has at least one first integrated circuit (IC) that is boundary-scan capable, and at least one second IC that is not boundary-scan capable, the equipment comprising:

an input for inputting files comprising a boundary scan description language (BSDL) file, a netlist and a connections list; and

a data structure generated from the BSDL file, the netlist and the connections list that defines all pins of the first IC that are capable of driving pins of the second IC and all pins of the first IC that are capable of reading pins of the second IC, whereby the second IC and its connections to the first IC can be tested by driving pins of the first IC using a test script that is specific to me second IC but independent of the first IC.

9. (original) Equipment according to claim 7 wherein the first IC has pins that are capable of adopting one of three states, being a high State, a low state and an input state.

10. (original) Equipment according to claim 7 wherein the first IC is connected to a boundary scan bus.

11. (original) Equipment according to claim 7, further comprising a parser and a compiler for parsing and compiling the BSDL file, the netlist and the connections list to generate the data structure, wherein the parser and compiler are implemented in computer programs loaded into a computer to be connected to the circuit to be tested.

12 (original). Equipment according to claim 11, wherein the computer further comprises a test script for testing the second IC and its connections to the first IC.

13. (original) Equipment according to claim 12, wherein the first IC has pins that are capable of adopting one of three states, being a high state, a low state and an input state, and wherein the test script is arranged to sequentially test whether a pin is in a read state by testing whether it can sequentially be driven into the low state and the high state.

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Canceled)

23.   (New) Circuit testing equipment for testing an integrated circuit board having a boundary scan test port, comprising:

a computer connectable to the boundary scan test port, the computer having a boundary scan description language file, a netlist, and a connections list loaded therein, the computer being adapted to compile these into a data structure for testing a circuit on the board and to receive a test script specific to an integrated circuit mounted on the board and to run the test script using the data structure to thereby send to the boundary scan test port selected signals to test selected pins of the integrated circuit.

24.   (New) The equipment of claim 23, wherein the test script is specific to the integrated circuit to be tested but independent of the circuit board on which it is mounted.

25.   (New) The circuit testing equipment according to claim 1, wherein the test script is also associated with other electrical components to be tested, including at least one of switches and light emitting diodes.